JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
ANANTHAPURAMU (A.P.)
COURSE STRUCTURE AND SYLLABUS
(For Affiliated Engineering Colleges w.e.f. 2017-18 Admitted Batch)

M.Tech-ECE-VLSI, VLSI SYSTEMS, VLSI SYSTEM DESIGN (VLSI, VLSIS, VLSISD)

M.Tech I Semester

S.No	Subject Code	Subject	L	T	P	C
1.	17D06101	Structural Digital System Design	4	-	-	4
2.	17D57101	Advanced MOSFET Modeling	4	-	-	4
3.	17D57102	CMOS Analog IC Design	4	-	-	4
4.	17D57103	CMOS Digital IC Design	4	-		4
5.	 17D57104 17D06103 17D57105	**Elective-I** a. VLSI Signal Processing b. Advanced Computer Architecture c. CAD for VLSI	3	-	-	3
6.	 17D06202 17D55206 17D57106	**Elective-II** a. CPLD and FPGA Architectures and Applications b. ASIC Design c. Optimization Techniques in VLSI Design	3	-	-	3
7.	17D38107	Structural Digital System Design Lab	-	-	3	2
8.	17D57107	VLSI System Design Lab - I	-	-	3	2
		Total	**22**	**-**	**06**	**26**

M.Tech II Semester

S.No	Subject Code	Subject	L	T	P	C
1.	17D57201	Low Power VLSI Design	4	-	-	4
2.	17D57202	CMOS Mixed signal Design	4	-	-	4
3.	17D06201	Embedded System Design	4	-	-	4
4.	17D06109	Test and Testability	4	-		4
5.	 17D55201 17D57203 17D57204	**Elective-III** a. System On Chip Architecture b. Semiconductor Memory Design and Testing c. RF IC Design	3	-	-	3
6.	 17D38202 17D55204 17D57205	**Elective-IV** a. Internet of Things b. Hardware and Software Co-design of Embedded System c. Physical Design Automation	3	-	-	3
7.	17D38208	Embedded System Design Lab	-	-	3	2
8.	17D57206	VLSI System Design Lab - II	-	-	3	2
		Total	**22**	**-**	**06**	**26**

M.Tech. II YEAR (III Semester)

S. No	Course Code	Subject	L	T	P	C
1.	17D20301 17D20302 17D20303	Elective – V (Open Elective) 1. Research Methodology 2. Human Values & Professional Ethics 3. Intellectual Property Rights	4	---	---	4
2.	17D57301	ELECTIVE – VI (MOOCs)	--	---	---	--
3.	17D57302	Comprehensive Viva Voce	--	---	---	2
4.	17D57303	Seminar	--	---	---	2
5.	17D57304	Teaching Assignment	--	---	---	2
6.	17D57305	Project Work Phase I	--	---	---	4
	Total		4			14

M.Tech. II YEAR (IV Semester)

S. No	**Course Code**	**Subject**	**L**	**T**	**P**	**C**
1.	17D57401	Project Work Phase II	--	---	---	12
	Total					**12**

Project Viva Voce Grades:

A: Satisfactory

B: Not Satisfactory

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D06101) STRUCTURED DIGITAL SYSTEM DESIGN

Course Objective:

- To study about structural functionality of different Digital blocks (Both combinational and Sequential)
- To provide an exposure to ASM charts, their notations and their realizations.
- To provide an exposure to VHDL and different styles of modeling using VHDL.
- To introduce the concept of micro programming and study issues related to micro programming

Course Outcome:

After Completion of this course, students will be able to

- Understand structural functionality of different digital blocks
- Represent and Realize their designs in ASM charts
- Represent their designs in different modeling styles by using VHDL
- Understand concept of Micro program and issues related to micro programming

UNIT-1

BUILDING BLOCKS FOR DIGITAL DESIGN: Multiplexer, Demultiplexer, Decoder, Encoder, Comparator, Adder, ALU, Carry-look-ahead adder.
BUILDING BLOCKS WITH MEMORY: Clocked building blocks, register building blocks, RAM, ROM, PLA, PAL, Timing devices.

UNIT –II

DESIGN METHODS: Elements of design style, top-down design, separation of controller and architecture, refining architecture, and control algorithm, Algorithmic State Machines, ASM chart notations.

UNIT-III

REALISING ASMS - Traditional synthesis from ASM chart, multiplexer controller method, one-shot method, ROM based method.
ASYNCHRONOUS INPUTS AND RACES - Asynchronous ASMs, Design for testability, test vectors, fault analysis tools.

UNIT-IV

MICROPROGRAMED DESIGN: Classical Microprogramming with Modem Technology; Enhancing the Control Unit; The 2910 Microprogram Sequencer; Choosing a Microprogram Memory; A Development System for Microprogramming; Designing a Microprogrammed Minicomputer

UNIT-V
MODELLING WITH VHDL: CAD tools, simulators, schematic entry, synthesis from VHDL.
DESIGN CASE STUDIES: Single pulse, system clock, serial to parallel data conversion, traffic light controller.

TEXT BOOKS:

1. Franklin P. Prosser and David E. Winkel, "The Art of Digital Design", Prentice Hall.
2. Roth, “Digital System Design using VHDL”, Mc. Graw Hill, 2000

REFERENCE BOOKS:

1. William Fletcher, An Engineering Approach to Digital Design, 1st Edition, Prentice-Hall India, 1997.
2. William J Dally and John W Poulton, Digital Systems Engineering, Cambridge University Press, 2008.
3. Jayaram Bhasker, A VHDL Primer, 3rd edition, Prentice-Hall India, 2009.
4. VHDL for Programmable Logic - Kevin Skahill, Cypress Semiconductors

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D57101) ADVANCED MOSFET MODELING

Course Outcomes:

After the completion of this course, student will be able to

- Derive mathematical models for modern MOS devices.
- Provide solution to overcome short channel issues.
- Create various compact models appropriate for industry.

UNIT I

BASIC DEVICE PHYSICS

Intrinsic and extrinsic semiconductors, direct and indirect semiconductors- Electrons and holes in silicon energy bands: electron and hole densities in equilibrium- Fermi Dirac statistics, carrier concentration, ionization of impurities. Carrier transport in silicon : drift current, diffusion current. pn junctions built in potential, electric field, current voltage characteristics.

UNIT II

MOSFET DEVICES

MOS capacitors surface potential- structure characteristics, electrostatic potential and charge distribution- threshold voltage- polysilicon work function- interface states and oxide traps. Long channel MOSFETs : threshold voltage, substrate bias and temperature dependence of threshold voltage, drain current model, subthreshold characteristics, channel mobility, capacitances.

UNIT III

NANO SCALED MOSFETs

Scaling of MOSFETs: Short channel MOSFETs – short channel effects, velocity saturation, channel length modulation, DIBL, GIDL. Variability in MOSFETs.Reliability of MOSFETs high field effects, hot carrier degradation, negative bias temperature instability, MOSFET breakdown, high k dielectrics. Non classical MOSFETs : SOI MOSFETs Current voltage equations, fully depleted SOI MOSFETs, partially depleted SOI MOSFETs, Heterostructure MOSFETs, strained channel MOSFETs, Power MOSFETs,SiC MOSFETs- Silicon Nanowires-Carbon Nanotubes.

UNIT IV

NOISE MODELING AND PROCESS VARIATION

Noise sources in MOSFET: Flicker noise modeling, Thermal noise modeling- model for accurate distortion analysis- nonlinearities in CMOS devices and modeling- calculation of distortion in analog CMOS circuits. Influence of process variation- modeling of device mismatch for Analog/RF Applications- Benchmark circuits for quality assurance- Automation of the tests.

UNIT V

COMPACT MODELS FOR CIRCUIT SIMULATORS

Introduction to compact models, SPICE Level 1, 2 and 3 MOS models, BSIM model, EKV model, High frequency models- Parameter extraction of MOSFETs.

TEXT BOOKS:

1. Taur and T. H. Ning, ―Fundamentals of Modern VLSI Devices‖, Cambridge University Press, Cambridge, United Kingdom, 1998.
2. TrondYtterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, ―Device Modeling for Analog and RF CMOS Circuit Design‖, John Wiley & Sons Ltd,2003.
3. B. G. Streetman and S. Banarjee, ―Solid State Electronic Devices 6th edition‖, Prentice Hall of India Pvt. Ltd, New Delhi, India, 2005.
4. N. DasGupta and A. DasGupta, ―Semiconductor Devices – Modeling and Technology‖, Prentice Hall of India Pvt. Ltd, New Delhi, India, 2004.

REFERENCE BOOKS:

1. A. B. Bhattacharyya, ―Compact MOSFET Models for VLSI Design‖, John Wiley & Sons Inc., 2009.
2. C. K. Maiti, N. B. Chakrabarti, S. K. Ray, "Strained silicon hetero structures: materials and devices‖, The Institution of Electrical Engineers, London, United Kingdom, 2001.
3. WeidongLiuandChemmingHu‖BSIM 4 and MOSFET Modeling for IC simulation‖, World scientific and Publishing Co. Pte. Ltd.2011

WEB REFERENCE BOOKS:

1. www.fairchildsemi.com/products/discretes/fets/
2. www.mosis.com/pages/Technical/Testdata/submicron-spice-parameters
3. en.wikipedia.org/wiki/Carbon_nanotube
4. www.nxp.com/wcm_documents/models/mos-models/model-9/aacd96_sel
5. web.cs.mun.ca/~paul/transistors/node3.html
6. www.elab.ntua.gr/bemos/index.html

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D57102) CMOS ANALOG IC DESIGN

Course Outcomes:

After completion of the course the students will be able to

- Understand significance of different biasing styles and apply them for designing analog ICs.
- Analyze the functionality of Current Mirrors, Current Sinks, Differential amplifiers and Current amplifiers.
- Design basic building blocks of analog ICs like, current mirrors, current sources, current sinks, two stage CMOS Power amplifiers and comparators.

UNIT –I

MOS Devices and Modeling: The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage REFERENCE BOOKS, Band gap Reference.

UNIT –III

CMOS Amplifiers: Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures, Mismatch-offset cancellation techniques, Reduction of Noise by offset cancellation techniques, Alternative definition of CMRR.

UNIT –IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT –V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce,
3. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D57103) CMOS DIGITAL IC DESIGN

Course Outcomes:

After completion of the course the students will be able to

- Design CMOS inverters with specified noise margins and propagation
- Complete knowledge regarding the different issues associated with organization and design of semiconductor memories
- Realize and implement basic combinational and sequential elements that are commonly observed in digital ICs.
- Design basic combinational and sequential elements using NMOS and CMOS design strategies.
- Analyze the dynamic performance of CMOS circuits

UNIT-I

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits: Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, 2nd Ed., PHI.

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D57104) VLSI SIGNAL PROCESSING
Elective-I

Course Outcomes:

After completion of the course the students will be able to

- Get in depth knowledge on signal processing system and various techniques of power reduction.
- Realize various adders, multipliers and filters and optimize their operation of by reducing the redundant operations
- Apply concept of pipelined architecture for various combinational and sequential circuit modules like adders, multipliers, filters
- Design Low Power IIR filters

UNIT-I

Transformations for retiming.Folding and unfolding DSP programs.

UNIT-II

Bit level arithmetic structures- parallel multipliers, interleaved floor plan and bit plan based digital filters. Bit serial multipliers. Bit serial filter design and implementation . Canonic signed digit arithmetic, Distributed arithmetic.

UNIT-III

Redundant arithmetic, redundant number representations , carry free radix 2 addition and subtraction . Hybrid radix 4 addition. Radix 2 hybrid redundant multiplication architectures , data format conversion. Redundant to nonredundant converter.Numerical strength reduction.

UNIT-IV

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining. Implementation of wave-pipelined systems.Asynchronous pipelining.

UNIT-V

Scaling versus power consumption. Power analysis, power reduction techniques, power estimation techniques. Low power IIR filter design .Low power CMOS lattice IIR filter.

TEXT BOOKS:

1. K.K. Parhi : VLSI Digital Signal Processing systems, John Wiley, 1999.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, YannisTsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D06103) ADVANCED COMPUTER ARCHITECTURE

Elective-I

Course Outcomes:

After completion of the course the students will be able to

- Know about different parallel computer models and their network properties.
- Understand about different concepts related to pipelining and super scalar techniques.
- Get complete knowledge regarding multi processors and multi computers.

UNIT - I

Parallel Computer Models – System attributes to performance, Multiprocessors and Multicomputers, Classifications of Architectures, Multivector and SIMD Computers, Architecture development tracks

UNIT - II

Program and Network Properties- Conditions for parallelism, Program partitioning and Scheduling, Program flow mechanisms, System interconnect architectures, Performance metrics and measures, Parallel Processing Applications

UNIT-III

Processors and Memory Hierarchy- Advanced Processor Technology, Superscalar and Vector processors, Memory hierarchy technology, Virtual Memory, Backplane bus systems, Cache memory organizations, Shared memory organizations

UNIT - IV

Pipelining and Superscalar Techniques Linear Pipeline processors, Nonlinear pipeline processors, Instruction pipeline design, Arithmetic pipeline design, Superscalar and Super Pipeline Design

UNIT- V

Multiprocessors and Multicomputers Multiprocessor System Interconnects, Cache Coherence and Synchronization mechanisms, Three generations of Multicomputers, Message passing mechanisms, Vector Processing principles, Principles of Multithreading

TEXT BOOKS:

1. Hwang kai, “Advanced Computer Architecture”, McGraw-Hill, 2001.
2. Patterson**,** Morgn Kaufmann, “Computer Architecture”,2001.

REFERENCE BOOKS:

1. William Stallings, Computer Organization and Architecture, 8th Edition, Prentice-Hall India, 2010.
2. David A Patterson and John L. Hennesey, Computer Organization and Design, 4th Edition, Elsevier India, 2011.
3. Andrew S Tanenbaum and James R Goodman, Structured Computer Organization, 5th Edition PrenticeHall India, 2009.

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D57105) CAD FOR VLSI
Elective-I

Course Outcomes:

After completion of the course the students will be able to

- Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- Practice the application of fundamentals of VLSI technologies
- Optimize the implemented design for area, timing and power by applying suitable constraints.
- Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on reconfigurable hardware platform (FPGA)
- Gain knowledge on the methodologies involved in design, verification and implementation of digital designs on MCMs.
- Develop various algorithms at various levels of physical design.

UNIT-I

VLSI Physical Design Automation VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT-II

Partitioning, Floor Planning, Pin Assignment and Placement Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.
Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT-IV

Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.
Global Routing and Detailed Routing Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT-V
Physical Design Automation of FPGAs and MCMs FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by NaveedShervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D06202) CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
Elective-II

Course Outcomes:

After completion of the course the students will be able to

- Acquire knowledge about various architectures and device technologies of PLD"s
- Comprehend FPGA Architectures
- Analyze System level Design and their application for Combinational and Sequential Circuits
- Get familiar with Anti-Fuse Programmed FPGAs
- Apply knowledge of this subject for various design applications

UNIT-I
Introduction to Programmable Logic Devices Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II
Field Programmable Gate Arrays Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT–III
SRAM Programmable FPGAs Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT–IV
Anti-Fuse Programmed FPGAs Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT–V
Design Applications General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:
1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

REFERENCE BOOKS:
1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier,Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D55206) ASIC DESIGN
Elective-II

Course Outcomes:

After completion of the course the student will be able to

- Understand different types of ASICs and their libraries.
- Understands about programmable Asics, I/O modules and their interconnects.
- Gets complete knowledge regarding different methods of software ASIC design their simulation, testing and construction of ASICs.

UNIT I

INTRODUCTION TO ASICs:

Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT II

PROGRAMABLE ASICS AND PROGRAMABLE ASIC LOGIC CELLS:

The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III

I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE:

DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT IV

LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS:

Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Senthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT V

SIMULATION, TEST AND ASIC CONSTRUCTION:

Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

TEXT BOOKS:

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L.J.Herbst, “Intigrated Circuit Engineering”, Oxford Science Publications, 1996.

REFERENCE BOOKS:

3. HimanshuBhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design compiler”, 2nd Edition, Kluwer Academic, 2001.

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D57106) OPTIMIZATION TECHNIQUES IN VLSI DESIGN
Elective-II

Course Outcomes:
After completion of the course the students will be able to

- Understand basics of statistical modeling
- Analyze performance of CMOS circuits with respect to power, area and speed
- Gets complete knowledge regarding the various algorithms used for optimization of power and area.

UNIT-I
Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT-II
Statistical Performance, Power and Yield Analysis Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III
Convex Optimization Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT-IV
Genetic Algorithm Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement GASP algorithm-unified algorithm.

UNIT-V
GA Routing Procedures and Power Estimation Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power -AshishSrivastava, Dennis Sylvester, David Blaauw, Springer, 2005.

2. Genetic Algorithm for VLSI Design, Layout and Test Automation -PinakiMazumder, E.Mrudnick, Prentice Hall,1998.

REFERENCE BOOKS:

1. Convex Optimization - Stephen Boyd, LievenVandenberghe, Cambridge University Press,2004.

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M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

(17D38107) STRUCTURAL DIGITAL SYSTEM DESIGN LAB

Course Objective:

- To understand about VHDL and Verilog Programming in all available styles.
- To understand differences between Verilog and VHDL.
- To represent the different digital blocks in verilog and VHDL in all available styles of modelling

Course Outcome:

After completion of this course the students will be able to understand

- Different modeling styles available in VHDL and Verilog and difference between them
- Difference between verilog and VHDL
- Representation of different digital modules in different modelling styles available in VHDL and Verilog

Using VHDL or Verilog do the following experiments

1. Design of 4-bit adder / subtractor
2. Design of Booth Multiplier
3. Design of 4-bit ALU
4. Design SISO, SIPO, PISO, PIPO Registers
5. Design of Ripple, Johnson and Ring counters
6. Design of MIPS processor
7. Design of Washing machine controller
8. Design of Traffic Light Controller
9. Design “1010” pattern detector using Mealy state Machine
10. Design “1100” recursive pattern detector using Moore state Machine
11. Design simple Security System Using FSM/ASM
12. Mini Project

Tools Required:

VHDL or VERILOG

Hardware Required:

Computers with latest Configuration.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year I Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
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(17D57107) VLSI SYSTEM DESIGN LAB - I

Learning Outcomes:

After completion of this course the students will be able to

- Understand syntax of various commands available with verilog and fundamental associated with design of digital systems
- To design and simulate and implement various digital system like traffic light controller, UART.
- Able develop problem solving skills and adapt them to solve real world problems
- Write scripts using perl for building digital blocks

The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

The students are required to design and implement the Layout of the following experiments of any SIX using CMOS 130nm Technology.

List of Experiments:

1. Inverter Characteristics.
2. Full Adder.
3. RS-Latch, D-Latch and Clock Divider.
4. Synchronous Counter and Asynchronous Counter.
5. Static RAM Cell.
6. Dynamic RAM Cell.
7. ROM
8. Digital-to-Analog-Converter.
9. Analog-to-Digital Converter.
10. “10101” pattern detector using Mealy FSM
11. Analytical Comparator.
12. Mini Project

Lab Requirements:

Software:

Xilinx ISE Suite, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Perl Software.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D57201) LOW POWER VLSI DESIGN

Course Outcomes:

After completion of this subject, students will be able to

- Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- Implement Low power design approaches for system level and circuit level measures.
- Design low power adders, multipliers and memories for efficient design of systems.

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	4	**0**	**0**	**4**

(17D57202) CMOS MIXED SIGNAL DESIGN

Course outcomes:

After the Completion of the course the students will be able to

- Demonstrate first order filter with least interference
- Extend the concept of phase locked loop for designing PLL application with minimum jitter by considering non ideal effects.
- Design different A/D, D/A, modulators, demodulators and different filter for real time applications

UNIT-I

Switched Capacitor Circuits Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT-II

Phased Lock Loop (PLL) Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT-III

Data Converter Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT-IV

Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT-V

Oversampling Converters Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibitquantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
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(17D06201) EMBEDDED SYSTEM DESIGN

Course Outcomes:

After completion of this course the students will be able to understand

- The issues relating to hardware and software design concepts associated with processor in Embedded Systems.
- The concept of low power microcontrollers.
- The hardware software co- design issues pertaining to design of an Embedded System using low power microcontrollers.

UNIT – I

Introductionto Embedded Electronic Systems and Microcontrollers:

An Embedded System-Definition, Embedded System Design and Development Life Cycle, An Introduction to Embedded system Architecture, The Embedded Systems Model, Embedded Hardware:The Embedded Board and the von Neumann Model, Embedded Processors: ISAArchitectureModels, Internal Processor Design, Processor Performance, Board Memory: Read-Only Memory (ROM), Random-Access Memory (RAM), Auxiliary Memory, Memory Management of External Memory and Performance, Approaches to Embedded Systems, Small Microcontrollers, Anatomy of a Typical Small Microcontroller, Small Microcontrollers Memory, Embedded Software, Introduction to small microcontroller (MSP430).

UNIT-II

MSP430 – I:

Architecture of the MSP430 Processor: Central Processing Unit, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Examples, Reflections on the CPU and Instruction Set, Resets, Clock System, Memory and Memory Organization.

Functions, Interrupts, and Low-Power Mode: Functions and Subroutines, Storage for Local Variables, Passing Parameters to a Subroutine and Returning a Result, Mixing C and Assembly Language, Interrupts, Interrupt Service Routines, Issues Associated with Interrupts, Low-Power Modes of Operation.

UNIT – III

MSP430 – II:

Digital Input, Output, and Displays: Parallel Ports, Digital Inputs, Switch Debounce, Digital Outputs, Interface between Systems, Driving Heavier Loads, Liquid Crystal Displays, Simple Applications of the LCD.

Timers: Watchdog Timer, Timer_A, Timer_A Modes, Timer_B,Timer_B Modes, Setting the Real-Time Clock, State Machines.

UNIT – IV

MSP430 Communication:

Communication Peripherals in the MSP430, Serial Peripheral Interface, SPI with the USI, SPI with the USCI, AThermometer Using SPI Modes,Inter-integrated Circuit Bus(I^2C) and its operations, State Machines for I^2C Communication, AThermometer Using I^2C, Asynchronous Serial Communication, Asynchronous Communication with the USCI_A, ASoftware UART Using Timer_A, Other Types of Communication.

UNIT – V

MSP430 Case Studies:

Introduction to Code Composer studio (CC Studio Ver. 6.1) a tutorial, A Study of blinking LED, Enabling LED using Switches, UART Communication, LCD interfacing, Interrupts, Analog to Digital Conversion, General Purpose input and output ports, I2C.

TEXT BOOKS:

1. Tammy Noergaard “Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers”, Elsevier(Singapore) Pvt.Ltd.Publications, 2005.
2. John H. Davies “MSP430 Microcontroller Basics”,Elsevier Ltd Publications, Copyright 2008.

REFERENCE BOOKS

1. Manuel Jiménez Rogelio,PalomeraIsidoroCouvertier “Introduction to Embedded SystemsUsing Microcontrollers and the MSP430” Springer Publications, 2014.
2. Frank Vahid, Tony D. Givargis, “Embedded system Design: A Unified Hardware/Software Introduction”, John Wily & Sons Inc.2002.
3. Peter Marwedel, “Embedded System Design”, Science Publishers, 2007.
4. Arnold S Burger, “Embedded System Design”, CMP Books, 2002.
5. Rajkamal, “Embedded Systems: Architecture, Programming and Design”, TMH Publications,Second Edition, 2008.

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
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(17D06109) TEST AND TESTABILITY

Course Outcomes:

After completion of this course the students will be able to

- Understand different types of faults associated with logic circuits and types of testing by employing fault models to the logic circuits.
- Study about different methods of simulation and algorithms associated with testing.
- Get complete knowledge about different methods of simulation and algorithms associated with testing.

UNIT-I: Introduction to Testing

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT-II: Logic and Fault Simulation

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT -III: Testability Measures

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT-IV: Built-In Self-Test

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT-V: Boundary Scan Standard

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits”, Kluwer Academic Pulishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.

REFERENCE BOOKS:

3. P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D55201) SYSTEM ON CHIP ARCHITECTURE
Elective-III

Course Outcomes:
After completion of this course the students will be able to

- Get complete basics related to SoC architecture and different approaches related to SoC Design.
- Able to select an appropriated robust processor for SoC Design
- Able to Select an appropriate memory for SoC Design.
- Design SoC
- Realize real time case studies

UNIT I:
Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II:
Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III:
Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV:
Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V:
Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:
1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
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(17D57203) SEMICONDUCTOR MEMORY DESIGN AND TESTING

Elective-III

Course Outcomes:

After completion of the course the students will be able to

- Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.
- Able to build fault models for memory testing.
- Analyze different parameters that leads malfunctioning of memories.
- Design reliable memories with efficient architecture to improve processes times and power

UNIT-I Random Access Memory Technologies SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II Non-volatile Memories Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-IV Semiconductor Memory Reliability and Radiation Effects General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT-V Advanced Memory Technologies and High-density Memory Packing Technologies Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.

2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma-2002, Wiley.

REFERENCE BOOKS:

1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice all.

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
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(17D57204) RF IC DESIGN

Course outcomes:

After completion of the course the students will be able to

- Demonstrate in-depth knowledge in Radio Frequency Integrated Circuits.
- Analyze complex engineering problems critically for conducting research in RF systems.
- Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
- Apply appropriate techniques to engineering activities in the field of RFIC Design.

UNIT – I: BASIC CONCEPTS IN RF DESIGN

Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

UNIT – II: TRANSCEIVER ARCHITECTURES

General considerations, Receiver Architectures-Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures-Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters, Other Transmitter Architectures.

UNIT -III: LNA AND MIXERS

General considerations, Problem of input matching, Low Noise Amplifiers design in various topologies, Gain Switching, Band Switching, Mixers-General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

UNIT – IV: OSCILLATORS

Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, LC VCOs with wide tuning range, phase noise, Mathematical model of VCOS, Quadrature Oscillators.

UNIT – V: PLL AND POWER AMPLIFIER

PLLS-Phase detector, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase noise in PLLs, Loop Bandwidth. Power Amplifiers-General considerations, Classification of power amplifiers, High-Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques.

TEXT BOOKS:

1. B.Razavi, “RF Microelectronics”, Prentice-Hall PTR, 2nd Edition, 1998.

REFERENCE BOOKS:

1. T.H.Lee, “The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd, 1998.
2. R.Jacob Baker, Harry W.Li, D.E. Boyce, “CMOS Circuit Design, Layout and Simulation”, Prentice-Hall of India, 1998.

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D38202) INTERNET OF THINGS
Elective-IV

Course Outcomes:
After completion of the course the student will be able to

- Able to understand the application areas of IOT
- Able to realize the revolution of Internet in Mobile Devices, Cloud &Sensor Networks
- Able to understand building blocks of Internet of Things and characteristics.

Unit I
Introduction & Concepts: Introduction to Internet of Things, Physical Design of IOT, Logical Design of IOT, IOT Enabling Technologies, IOT Levels.

Unit II
Domain Specific IOTs: Home Automation, Cities, Environment, Energy, Retail, Logistics, Agriculture, Industry, Health & Life Style.

Unit III
M2M & System Management with NETCONF-YANG: M2M, Difference between IOT and M2M, SDN and NFV for IOT, Software defined Networking, Network Function Virtualization, Need for IOT Systems Management, Simple Network Management Protocol, Limitations of SNMP, Network Operator Requirements, NETCONF, YANG, IOT Systems management with NETCONF-YANG.

Unit IV
Developing Internet of Things & Logical Design using Python: Introduction, IOT Design Methodology, Installing Python, Python Data Types & Data Structures, Control Flow, Functions, Modules, Packages, File Handling, Date/ Time Operations, Classes, Python Packages.

Unit V
IOT Physical Devices & Endpoints: What is an IOT Device, Exemplary Device, Board, Linux on Raspberry Pi, Interfaces, and Programming& IOT Devices.

TEXT BOOKS:
1. VijayMadisetti, ArshdeepBahga," Internet of ThingsA Hands-On- Approach",2014, ISBN:978 0996025515

REFERENCE BOOKS:
1. AdrianMcEwen, "Designing the Internet of Things", Wiley Publishers, 2013, ISBN:978-1-118-43062-0
2. Daniel Kellmereit, "The Silent Intelligence: The Internet of Things". 2013, ISBN0989973700

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
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(17D55204) HARDWARE AND SOFTWARE CO-DESIGN OF EMBEDDED SYSTEM
Elective-IV

Course outcomes:
After completion of this course the students will be able to

- Analyze and apply design methodologies.
- Appreciate the fundamental building blocks of the using hardware and software co-design and related implementation and testing environments and techniques and their interrelationships.
- Get familiar with modern hardware/software tools for building prototypes and to be able to demonstrate practical competence in these areas

UNIT I NATURE OF HARDWARE AND SOFTWARE
Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Transformations.

UNIT II DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE
Software Implementation of Data Flow – Converting queues and actors into software, Dynamic Scheduler – Hardware Implementation of Data Flow – single rate SDF graphs into hardware, Pipelining – Analysis of control flow and data flow – construction of control and data flow graph – Translating C into hardware – Designing data path and controller.

UNIT III DESIGN SPACE OF CUSTOM ARCHITECTURES
Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT IV HARDWARE/ SOFTWARE INTERFACES
Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer‟s model.

UNIT V CASE STUDIES TriviumCripto coprocessor – Trivium stream cipher algorithm, Trivium for 8-bit platforms – AES coprocessor, CORDIC coprocessor – algorithm and implementation.

1. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf, ”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub, 1997.

REFERENCE BOOKS:

1. Giovanni De Micheli, Rolf Ernst Morgon, ”Reading in Hardware/Software Co-Design“ Kaufmann Publishers, 2001.
2. Patrick Schaumont, A Practical Introduction to Hardware/Software Codesign, 2nd Edition, Springer, 2010.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**

(17D57205) PHYSICAL DESIGN AUTOMATION

Elective-IV

Course Outcomes:

After completion of the course the students will be able to

- Understand relation between automation algorithms and constraints posed by VLSI technology.
- Adopt algorithms to meet critical design parameters.
- Design area efficient logics by employing different routing algorithms and shape functions
- Simulate and synthesis different combinational and sequential logics

UNIT-I

VLSI design automation tools: algorithms and system design. Structural and logic design. Transistor level design.Layout design.Verification methods. Design management tools.

UNIT-II

Layout compaction, placement and routing, Design rules, symbolic layout. Applications of compaction.Formulation methods.Algorithms for constrained graph compaction.Circuit representation. Wire length estimation. Placement algorithms.Partitioning algorithms.

UNIT-III

Floor planning and routing: floor planning concepts. Shape functions and floor planning sizing. Local routing.Area routing.Channel routing, global routing and its algorithms.

UNIT-IV

Simulation and logic synthesis: gate level and switch level modeling and simulation. Introduction to combinational logic synthesis.ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

UNIT-V

High-level synthesis: hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

TEXT BOOKS:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley ,1998.
2. N.A.Sherwani , Algorithms for VLSI Physical Design Automation, (3/e), Kluwer,1999.

REFERENCE BOOKS:

1. S.M. Sait , H. Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

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M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
	0	**0**	**3**	**2**

(17D38208) EMBEDDED SYSTEM DESIGN LAB

Course Outcomes:

After Completion of this Lab, Students will be able to

- Design and Implement basic circuits that are used in Embedded systems.
- Develop code using appropriate tools.
- Test the circuit performance with standard benchmark circuits.

List of Experiments

PART – A

Using Embedded C

Note: Any 10 Programs form the following

1. Write a simple program to print "hello world"
2. Write a simple program to show a delay.
3. Write a loop application to copy values from P1 to P2
4. Write a c program for counting the no of times that a switch is pressed & released.
5. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.
6. Write a program to create a portable hardward delay.
7. Write a c program to test loop time outs.
8. Write a c program to test hardware based timeout loops.
9. Develop a simple EOS showing traffic light sequencing.
10. Write a program to display elapsed time over RS-232 link.
11. Write a program to drive SEOS using Timer 0.
12. Develop software for milk pasteurization system.

PART – B

Note. Any 6 Programs from the following (Experiment – 1 is mandatory)

1. A Study of Code Composer Studio (CC Studio Latest Version)
2. Flashing a light by a software delay.
3. Displaying Characters on LCD.
4. Serial Communication using UART.
5. Basic Input and Output using MSP430 UART.
6. Interrupt Handling using MSP430.
7. Analog to Digital Conversion using MSP430.
8. Interfacing external Devices to GPIO Ports

Equipments Required:

1. Computers with latest configuration.
2. Code Composer Studio v6.1 (Preferably Latest version)
3. MSP430/ARM based Hardware kits and add-on boards.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech I year II Semester (VLSI SYSTEM DESIGN)	**L**	**T**	**P**	**C**
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(17D57206) VLSI SYSTEM DESIGN LAB - II

Course Outcomes:

The students are required to perform any Six of the following experimental concepts with suitable complexity mixed-signal application based circuits o (circuits consisting of both analog and digital parts) using necessary software tools.

List of experimental Concepts:

1. Analog circuit simulation.
2. Digital circuit simulation.
3. Mixed signal simulation.
4. Layout Extraction.
5. Parasitic values estimation from layout
6. Layout Vs Schematic.
7. Net List Extraction.
8. Design Rule Checks.

Lab Requirements:

Software: Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Mentor Graphics Back End/Tanner Software tool, Mixed Signal simulator

Hardware: Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

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M.Tech III semester (VLSI SYSTEM DESIGN) **L T P C**

4 0 0 4

(17D20301) RESEARCH METHODOLOGY
(Elective V-OPEN ELECTIVE)

UNIT I

Meaning of Research – Objectives of Research – Types of Research – Research Approaches – Guidelines for Selecting and Defining a Research Problem – research Design – Concepts related to Research Design – Basic Principles of Experimental Design.

UNIT II

Sampling Design – steps in Sampling Design –Characteristics of a Good Sample Design – Random Sampling Design.
Measurement and Scaling Techniques-Errors in Measurement – Tests of Sound Measurement – Scaling and Scale Construction Techniques – Time Series Analysis – Interpolation and Extrapolation.
Data Collection Methods – Primary Data – Secondary data – Questionnaire Survey and Interviews.

UNIT III

Correlation and Regression Analysis – Method of Least Squares – Regression vs Correlation – Correlation vs Determination – Types of Correlations and Their Applications

UNIT IV

Statistical Inference: Tests of Hypothesis – Parametric vs Non-parametric Tests – Hypothesis Testing Procedure – Sampling Theory – Sampling Distribution – Chi-square Test – Analysis of variance and Co-variance – Multi-variate Analysis.

UNIT V

Report Writing and Professional Ethics: Interpretation of Data – Report Writing – Layout of a Research Paper – Techniques of Interpretation- Making Scientific Presentations in Conferences and Seminars – Professional Ethics in Research.

Text Books:

Research Methodology:Methods And Techniques – C.R.Kothari, 2nd Edition,New Age International Publishers.
Research Methodology: A Step By Step Guide For Beginners- Ranjit Kumar, Sage Publications (Available As Pdf On Internet)
Research Methodology And Statistical Tools – P.Narayana Reddy And G.V.R.K.Acharyulu, 1st Edition,Excel Books,New Delhi.

REFERENCES:

1. Scientists Must Write - Robert Barrass (Available As Pdf On Internet)
2. Crafting Your Research Future –Charles X. Ling And Quiang Yang (Available As Pdf On Internet)

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M.Tech III semester (VLSI SYSTEM DESIGN) **L T P C**

4 0 0 4

(17D20302) HUMAN VALUES AND PROFESSIONAL ETHICS
(Elective V-OPEN ELECTIVE)

UNIT I:

HUMAN VALUES:Morals, Values and Ethics-Integrity-Work Ethic-Service learning – Civic Virtue – Respect for others – Living Peacefully – Caring – Sharing – Honesty - Courage- Co Operation – Commitment – Empathy –Self Confidence Character – Spirituality.

UNIT II:

ENGINEERING ETHICS: Senses of Engineering Ethics- Variety of moral issues – Types of inquiry – Moral dilemmas – Moral autonomy –Kohlberg‟s theory- Gilligan‟s theory- Consensus and controversy – Models of professional roles- Theories about right action- Self interest - Customs and religion –Uses of Ethical theories – Valuing time –Co operation – Commitment.

UNIT III :

ENGINEERING AS SOCIAL EXPERIMENTATION: Engineering As Social Experimentation – Framing the problem – Determining the facts – Codes of Ethics – Clarifying Concepts – Application issues – Common Ground - General Principles – Utilitarian thinking respect for persons.

UNIT IV:

ENGINEERS RESPONSIBILITY FOR SAFETY AND RISK: Safety and risk – Assessment of safety and risk – Risk benefit analysis and reducing riskSafety and the Engineer- Designing for the safety- Intellectual Property rights(IPR).

UINIT V:

GLOBAL ISSUES: Globalization – Cross culture issues- Environmental Ethics – Computer Ethics – Computers as the instrument of Unethical behavior – Computers as the object of Unethical acts – Autonomous Computers- Computer codes of Ethics – Weapons Development - Ethics .

Text Books :

1. “Engineering Ethics includes Human Values” by M.Govindarajan, S.Natarajan and V.S.SenthilKumar-PHI Learning Pvt. Ltd-2009.
2. “Engineering Ethics” by Harris, Pritchard and Rabins, CENGAGE Learning, India Edition, 2009.
3. “Ethics in Engineering” by Mike W. Martin and Roland Schinzinger – Tata McGrawHill– 2003.
4. “Professional Ethics and Morals” by Prof.A.R.Aryasri, Dharanikota Suyodhana-Maruthi Publications.
5. “Professional Ethics and Human Values” by A.Alavudeen, R.Kalil Rahman and M.Jayakumaran , Laxmi Publications.

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M.Tech III semester (VLSI SYSTEM DESIGN) **L T P C**

4 0 0 4

(17D20303) INTELLECTUAL PROPERTY RIGHTS
(Elective V-OPEN ELECTIVE)

UNIT – I

Introduction To Intellectual Property: Introduction, Types Of Intellectual Property, International Organizations, Agencies And Treaties, Importance Of Intellectual Property Rights.

UNIT – II

Trade Marks : Purpose And Function Of Trade Marks, Acquisition Of Trade Mark Rights, Protectable Matter, Selecting And Evaluating Trade Mark, Trade Mark Registration Processes.

UNIT – III

Law Of Copy Rights : Fundamental Of Copy Right Law, Originality Of Material, Rights Of Reproduction, Rights To Perform The Work Publicly, Copy Right Ownership Issues, Copy Right Registration, Notice Of Copy Right, International Copy Right Law.

Law Of Patents : Foundation Of Patent Law, Patent Searching Process, Ownership Rights And Transfer

UNIT – IV

Trade Secrets : Trade Secrete Law, Determination Of Trade Secrete Status, Liability For Misappropriations Of Trade Secrets, Protection For Submission, Trade Secrete Litigation.

Unfair Competition : Misappropriation Right Of Publicity, False Advertising.

UNIT – V

New Development Of Intellectual Property: New Developments In Trade Mark Law ; Copy Right Law, Patent Law, Intellectual Property Audits.

International Overview On Intellectual Property, International – Trade Mark Law, Copy Right Law, International Patent Law, International Development In Trade Secrets Law.

TEXT BOOKS & REFERENCES:

1. Intellectual Property Right, Deborah. E. Bouchoux, Cengage Learing.
2. Intellectual Property Right – Nleashmy The Knowledge Economy, Prabuddha Ganguli, Tate Mc Graw Hill Publishing Company Ltd.,